REMARKS/ARGUMENTS

In response to the Office Action mailed April 15, 2005, Applicants propose to amend their application and request reconsideration in view of the proposed amendment and the following remarks. It is proposed to cancel claims 2 and 3, leaving claims 1 and 4 pending.

The invention is directed to an integrated circuit that is particularly useful at frequencies that are used in cellular telephones and other communication apparatus. It is an important objective, in this kind of electronic equipment, to minimize power consumption. Thus, in amplifiers employed in that equipment, the voltage supplied to drive an amplification element, such as a transistor, may be switched between different values depending upon the power output of the amplification element. The invention provides a substantial improvement in this kind of circuitry by interconnecting a power source supplying a voltage to a circuit providing a bias to the semiconductor amplification element and the power source supplying a driving voltage to the amplification element.

For example, turning to the embodiment of Figure 1, when a relatively low voltage is applied at the power source 7 connected to the transistor Q1, transistor Q5 in an emitter follower circuit is essentially disabled so that the current flowing to the base of the transistor Q1 is reduced. When the higher power source voltage is applied at terminal 7 in Figure 1, then the transistor Q5 is active and functions as part of the bias circuit 40. This result occurs only because of the interconnection of the first and second power sources 7 and 6 by virtue of the transistor Q5 and the resistor R3 in the embodiment of Figure 1.

Figure 2 provides a different interconnection that brings about the same result. In the embodiment of Figure 2, a diode D2 is connected between the first power source 7 and the second power source 6 of the biasing circuit 50. Thus, as described at pages 8 and 9 of the patent application, at the time the bias from the first power source is relatively high, a bias current is supplied to the transistor Q4 through the diode D2. This current flow occurs because the voltage of the first power source 7 biases the diode D2 above its threshold voltage. On the other hand, when the voltage from the first power source 7 is low, i.e., the bias across the diode D2 is at or below the threshold voltage of the diode D2, that diode does not conduct so that the collector bias of the transistor Q4 is supplied solely from the second power source 6. Thus, in this state, the transistor Q4 supplies relatively little current to the amplification transistor Q1, conserving power.

Claim 3 was stated to be allowable if rewritten in independent form. That step is proposed. Amended claim 1 incorporates the limitation of examined claim 3. Therefore, amended claim 1 and its dependent claim 4, the only remaining claims, should be allowed.

Since this Amendment places the application in form for allowance, its entry and allowance of claims 1 and 4 are earnestly solicited.

Respectfully submitted,

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Date: June 9, 2005
JAW/tps

Amendment or ROA - Final (Revised 4/18/05)